LARGE SIGNAL DESIGN OF BROADBAND MONOLITHIC MICROWAVE FREQUENCY DIVIDERS

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ABSTRACT

A monolithic regenerative divider by two with a 6 GHz central input frequency has been designed and fully characterized using an improved harmonic balance formulation, suitable to deal with autonomous and phase-locked regimes. The solution paths when the input generator power and frequency are modified have been traced. The output power at the divided frequency has been evaluated as a function of both parameters as well as the output power of the free running oscillator regime. Every result has been experimentally verified observing an excellent agreement.

INTRODUCTION

The frequency dividers are essential devices of microwave communications systems. They are frequently included in phase locked loops, frequency synthetizers and frequency modulation devices.

There exist two types of frequency dividers based upon two different principles of operation. Static frequency dividers realize a cycle by cycle frequency division and are, inherently, very broadband. Dynamic or parametric frequency dividers are based upon the frequency regenerative properties of a circuit containing a non linear device and a feedback loop. These frequency dividers can be realized with varactors [1] or with transistors [2]. Such dividers have a limited bandwidth, however their simplicity and their ability to perform frequency division up to milimeter waves make them very attractive for communications purposes.

The design of monolithic frequency dividers requires a nonlinear analysis of the whole device. This analysis is based on the Harmonic Blance (HB) technique [3] [4]. Since the frequency dividers are intrinsically synchronized devices, a full nonlinear analysis must be able to handle the synchronization phenomenon.

In this paper we propose a full nonlinear analysis of a 6 to 3 GHz monolithic frequency divider. An improved formulation of the H.B. equation has been used, allowing to handle po-tentially unstable circuits, to obtain the synchro-nization band and the range of input powers for which frequency division occurs. This formulation includes the introduction of properly chosen probes to calculate autonomous regimes. A monolithic circuit has been built at the THOMSON foundry and the measured and simulated results have been compared with very a good accuracy.

DIVIDER CONCEPTION

The regenerative divider consists of an oscillator circuit with one of its harmonic compo-nents phase locked to an external input signal, being this oscillation quenched in the absence of injection. The division rate corresponds to the index of the locked harmonic component.

The working principle is based on a closed loop (Fig.1) in which the output signal at the divided frequency is fed-back and mixed with the external signal to produce a lower sideband at the divided frequency, which will be filtered, amplified and taken again to the mixer through the feed-back block.

The minimum input level necessary to get the frequency division depends on the loop total gain. As this gain increases the division can be obtained from lower input levels but care must be taken not to lead the circuit to unstability. Without an input signal the loop gain must be less than unity in order to avoid undesired oscillations.

When using a FET transistor in the design we can take advantage of its nonlinear behaviour to perform the mixing and amplifiying functions. External linear networks will be tasked with the filtering and the feed-back. Depending on the feed-back block connection, series or parallel configurations can be obtained.

A first step in the design will be obtaining the oscillation circuit at the desired output frequency. In the absence of the input signal this oscillation may be quenched by reducing the transistor gain or the feedback amount. The gain may be easily controlled by the gate dc voltage, which leads to biasing the transistor near pinchoff. In this region the quasi-quadratic characteristic of the nonlinear source I_{DS} is also very suitable for the mixing function.

The second step will be the optimization of the linear networks in order to match the transistor input port at the generator frequency and to allow only the presence of the divided frequency at the load. The feedback network only works at the divided frequency.

Because of its conception itself, the regenerative divider is prone to parasitic oscillations which makes necessary the stability analysis of both the bias point, and of the obtained solution as this latter may be synchronous (phase sensitive) or asynchronous (phase insensitive). Only the first one will be stable.

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ANALYSIS METHOD

The harmonic balance equation for the nonlinear circuit can be written as a nonlinear system of N equations in N variables:

$$H(X) = [Ax]\,X - [Ay]\,Y(X) - [Ag]\,G = 0 \quad (1)$$

where the vectors **X, Y, G** contain, respectively, the harmonic components of every command of the nonlinearities, the harmonic components of every nonlinearity and the independent generators values at their corresponding harmonic frequencies. The linear matrices [Ax], [Ay], [Ag] are obtained from the embedding circuit and, as it is shown, the vector **Y** depends nonlinearly on **X**.

In the case of autonomous circuits as in the case of frequency dividers some additionnal constraints must be brought to equation (1). When applying HB equation to an autonomous circuit the operating frequency is an unknown of the problem and we can set the phase of a frequency component to zero to obtain a system of N equations in N unknowns. In the case of a frequency divider the problem is slightly different as in this case the frequency of operation is known but the phase of the oscillation at the divided frequency has to be determined. In these two cases, applying Newton's method without any precaution leads most frequently to a convergence towards the trivial solution [5].

We overcome this difficulty by introducing a measurement probe in the circuit. Depending of the circuit's structure we use a voltage probe included in parallel with the load or a current probe included in series with the load as shown in fig-2. The criteria used for the choice of one particular probe are beyond the scope of this paper and will be discussed elsewhere.

The probe is set at the frequency ω_p with an amplitude |P| and a phase ϕ_p. A filter allows to eliminate the probe at all the other frequencies. In order not to perturb the initial circuit the admittance of the voltage probe or the impedance of the current probe must be zero, leading thus to a constraint nonlinear equation which must be added to the system (1).

$$H_p(|P|, \phi_p, \omega_p) = 0 \quad (2)$$

- For a free-running oscillator the phase ϕ_p is set to zero and the combination of equations (1) and (2) leads to a well conditionned nonlinear system of N+2 equations in N+2 unknowns.

- For a frequency divider ω_p is equal to the divided frequency. In this case the phase ϕ_p has to be determined by the same set of equations.

When one of the circuit parameters, such as the input generator power or its frequency, is modified the circuit behaviour is determined by tracing the solution path and by analyzing the stability of the solution along this path. This can be done by introducing the corresponding parameter μ in the harmonic balance equation.

$$\mathbf{H(X, \mu) = 0} \quad (3)$$

The stability of the solution of eq (3) for a parameter value can be checked with the aid of the characteristic equation obtained for a complex perturbation frequency $(\sigma + j\omega)$ [3]

$$[Ax]\,\Delta\mathbf{X} + [Ay]\,[U]\,\Delta\mathbf{X} = 0 \quad (4)$$

where the matrix [U] is the matrix of the partial derivatives of the non linear sources (conductances, transconductances and capaci-tances). Eq (4) can be rewritten as:

$$[J(\mathbf{X}, \mu, \sigma+j\omega)]\,\Delta\mathbf{X} = 0 \quad (5)$$

In the general case the stability is determined by plotting the Nyquist locus of :

$$\Delta(\mathbf{X}, \mu, \omega) = \det\,\{J(\mathbf{X}, \mu, j\omega)\}$$

but in the case of a divider by two, being $2f_0$ the input generator frequency, we can evaluate the system (5) for σ=0 along the solution path. Indeed it is possible to separate (5) into two subsystems corresponding respectively to the even and odd harmonic components:

$$\begin{bmatrix} J_{2p+1} & 0 \\ 0 & J_{2p} \end{bmatrix} \begin{bmatrix} \Delta X_{2p+1} \\ \Delta X_{2p} \end{bmatrix} = 0 \quad (6)$$

where J_{2p+1} and J_{2p} are respectively the odd and even subsystem jacobian matrixes.

Starting from a stable multiplicative regime with all the odd frequency components equal to zero, the determinants of these two submatrixes are evaluated along the solution path. A zero of the even determinant indicates the existence of a Direct type bifurcation, [3] while a zero of the odd determinant indicates an Inverse type bifurcation with the rise of a frequency divided regime.

With the help of the probe it is possible to start the divided solution. In this case the probe frequency will be fixed at that of the input generator divided by two and the variables to determine will be X, |P| and ϕ_p. Once the solution has been obtained for a parameter value the probe may be suppressed using the 'path following' method to trace the complete divided path.

RESULTS

Taking into account the previous considerations, a monolithic broadband frequency divider by two with an input frequency 6 GHz has been designed. The MESFET transistor is a TA5446 with a total gate width of 600 µm and a gate lenght of 0.5 µm. The complete circuit diagram appears in Fig.3. The linear elements are modelled with their parasitics provided by the foundry.

In the transistor model four nonlinearities are taken into account. They are the input diode current Igs, the input diode charge Qgs, the drain current Ids and the breakdown current Idg. The Tajima model [6] is used for Ids current and model parameters have been obtained through a fitting program, using the measurements from a pulse measurement system.

In order to obtain the bias range for which the circuit is able to oscillate without injected signal, a bias stability analysis after the Nyquist criterium has been performed. This analysis has been confirmed by the analysis of the autonomous solution for various gate bias voltages. The oscillation frequencies obtained for different gate bias are shown in Fig.4a, where they may be compared with the experimental results. The varia-tion of the oscillator output power with the bias gate voltage is given in Fig.4b, observing an excellent agreement with the experimental points. The power fall for VGS=-1.4 v constitutes the limit between the free running oscillation region and the stable bias region adequate for the frequency division.

At the stable bias point VGS=-1.6 v, VDS=3 v the circuit has been injected with a 5.8 GHz input signal. The frequency division is obtained from about 3 dBm input power and, starting the divided solution with the help of a probe, the curve output power versus input power (Fig.5) may be traced.

For a constant input level above the minimum necessary for the frequency division, the divider synchronization curve may be traced by varying the generator frequency. In this way the curve in Fig.6 has been obtained for 15 dBm input power. The resulting synchronization bandwidth is 400 MHz with an output power between 10 and 12 dBm.

CONCLUSIONS

A full nonlinear analysis of a monolithic frequency divider has been performed and results of simulation have been compared with experimental ones with a very good accuracy. The analysis method presented here allows to obtain the frequency bandwidth of the divider as well as the input power range needed for a frequency division. Frequency jumps and hysteresis phenomenons often encountered in such devices can be fully analyzed providing thus an useful tool for a deep investigation of synchronized devices.

ACKNOWLEDGEMENT

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REFERENCES

[1] *R.G.Harrison,* 'A Broadband Frequency Divider Using Microwave Varactors'. IEEE Trans. MTT Dec 1977 pp.1055-1059

[2] *C.Rauscher,* 'Regenerative Frequency Division with a GaAs FET', IEEE Transactions on MTT, Vol.32, n° 11 November 1984 pp.1461-1468

[3] *V. Rizzoli,A. Neri* "State of the art and present trends in nonlinear microwave CAD techniques" IEEE Trans Micowave Theory and Techn. Vol 36 n° 2 February 1988 pp.343-365

[4]*D.Hente, R.H.Jansen,* 'Frequency Domain Continuation Method for the Analysis and Stability Investigation of Nonlinear Microwave Circuits'. Proceeding IEEE pt H vol. 133, pp.551-362, Oct. 1986.

[5] *R. J Gilmore, M.B Steer*: " Nonlinear circuit analysis using the method of harmonic balance - A review of the Art - Part II. Advanced Concepts" International Journal of Microwave and Millimeter-Wave Computer-Aided engineering vol 1 n°2 April 1991 pp.143-158

[6] *C. Guo, M. Camiade, D. Rousset, A. Cessey, J. Obregon, A. Bert*: "Optimum design of non linear power FET amplifiers" IEEE Trans. on Microwave Theory Tech. Vol MTT 35 n°12 December 1987 pp.1348-1354

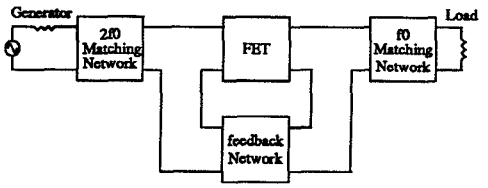

Fig.1 Block Diagram of a FET Divider

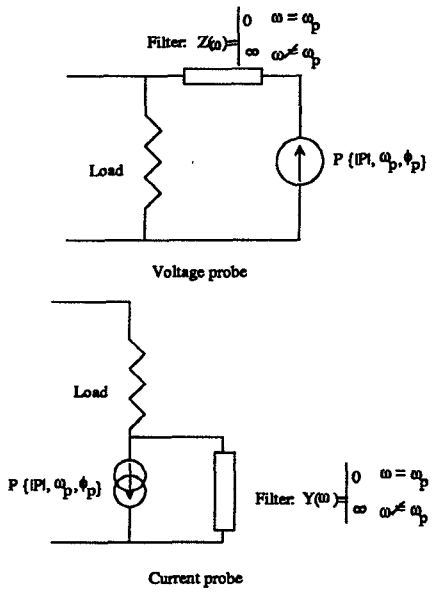

Fig-2 Inclusion of a voltage probe and a current probe in the circuit

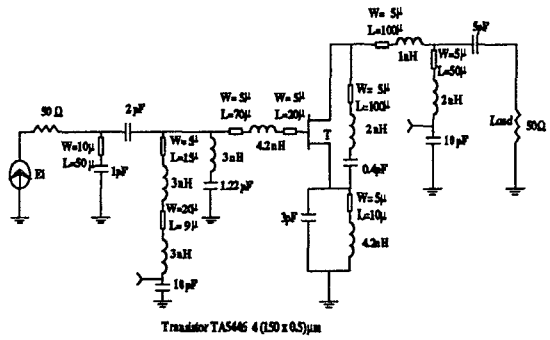

Fig 3 Complete circuit diagram of the monolithic frequency divider

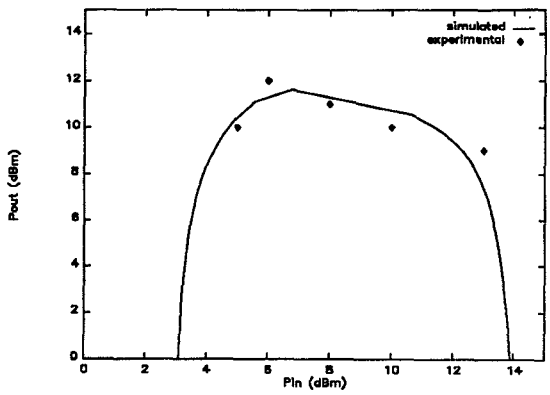

Fig 5 Output power of the frequency divider at f_0 versus the input power at $2f_0$ (Vg= -1.6 V; Vd= 3.0V)

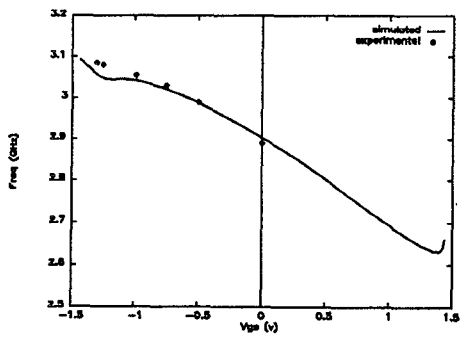

Fig 4-a Frequency of the oscillation versus the gate voltage (Vd=3.0V)

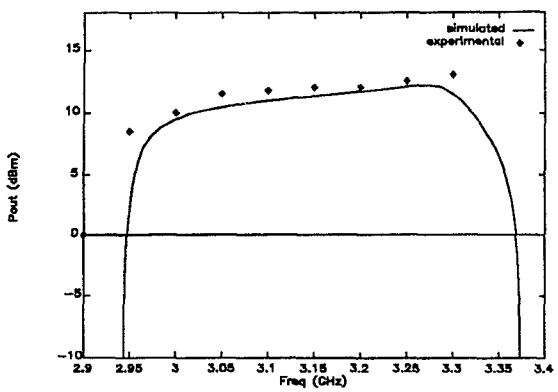

Fig.6 Output Power versus output frequency for 15 dBm input power (Vg=-1.6V ; Vd=3.0V)

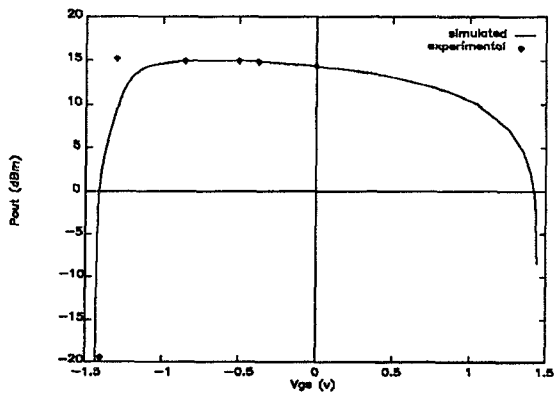

Fig 4-b Output power of the oscillator vs gate voltage (Vd=3.0V)